Amendments to the Claims:

The following listing of claims will replace all prior versions and/or listings of claims in the application.

Listing of Claims:

1. (Currently Amended) In an isochronous electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter of a plurality of local time counters, a method for determining a global ordering of events, said method comprising:

detecting an event associated with one of said plurality of chips;

generating a timestamp with said local time counter at the time of the occurrence of said detected event, said timestamp being associated with said event; ~~and~~

comparing said event and a normalized form of said timestamp with other events and associated normalized timestamps to determine an order of occurrence;

providing a Time Base selected by said processor, said Time Base being a baseline time value; and

transmitting a reset instruction from said processor to said plurality of local time counters associated with said plurality of chips, said plurality of local time counters resetting to a designated time so as to be synchronized with respect to each other;

wherein the transmitting of the reset instruction is staggered so as to ensure that said resetting occurs simultaneously, said transmitting taking into account delays caused by network topology.

2. (Cancelled)

3. (Currently Amended) The method of claim ~~2 where~~ 1 wherein said processor maintains a record of an offset between the reset local time counter time and the Time Base.

4. (Currently Amended) The method of claim ~~2~~ 1 wherein said designated time is the Time Base and said plurality of local time counters are reset so as to indicate the same time as said Time Base.

5. (Currently Amended) The method of claim ~~2~~ 1 wherein said transmitting of said reset instruction is performed using a simultaneous multicast write operation performed by said processor.

6. (Cancelled)

7. (Currently Amended) The method of claim ~~2~~ 1, further comprising:

resetting all of said plurality of chips and an additional chip, said resetting being performed to add the additional chip that is synchronized with said plurality of chips.

8-21. (Cancelled)

22. (Currently Amended) In an electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter of a plurality of local time counters, a storage medium comprising computer-executable instructions for a method comprising:

detecting an event associated with one of said plurality of chips;

generating a timestamp with said local time counter at the time of the occurrence of said detected event, said timestamp being associated with said event; ~~and~~

comparing said event and a normalized form of said timestamp with other events and associated normalized timestamps to determine an order of occurrence;

providing a Time Base selected by said processor, said Time Base being a baseline time value; and

transmitting a reset instruction from said processor to said plurality of local time counters associated with said plurality of chips, said plurality of local time counters resetting to a designated time so as to be synchronized with respect to each other;

wherein the transmitting of the reset instruction is staggered so as to ensure that said resetting occurs simultaneously, said transmitting taking into account delays caused by network topology.

23. (Cancelled)

24. (Currently Amended) The storage medium of claim ~~23~~ 22 where said processor maintains a record of an offset between the reset value of the local time counter and the Time Base.

25. (Currently Amended) The storage medium of claim ~~23~~ 22 wherein said designated time is the Time Base and said plurality of local time counters are reset so as to indicate the same time as said Time Base.

26. (Currently Amended) The storage medium of claim ~~23~~ 22 wherein the transmitting of said reset instruction is performed using a simultaneous multicast write operation performed by said processor.

27. (Cancelled)

28. (Currently Amended) The medium of claim ~~23~~ 22, wherein said method further comprises:

resetting all of said plurality of chips and an additional chip-, said resetting being performed to add the additional chip that is synchronized with said plurality of chips.

29-37. (Cancelled)

38. (New) In an isochronous electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter of a plurality of local time counters, a method for determining a global ordering of events, said method comprising:

detecting an event associated with one of said plurality of chips;

generating a timestamp with said local time counter at the time of the occurrence of said detected event, said timestamp being associated with said event;

comparing said event and a normalized form of said timestamp with other events and associated normalized timestamps to determine an order of occurrence;

providing a Time Base selected by said processor, said Time Base being a baseline time value;

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

transmitting each said offset for a local time counter to the chip with which the local time counter is associated;

recording each offset associated with each said local time counter at a location accessible to the chip associated with the local time counter; and

normalizing said timestamp using said offset associated with the local time counter prior to reporting said timestamp and said event to said processor.

39. (New) The method of claim 38 wherein a software timestamp received from an operating system is associated with said reported event and timestamp.

40. (New) The method of claim 39 wherein said software timestamp is used in determining said order of occurrence of events.

41. (New) In an electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter of a plurality of local time counters, a storage medium comprising computer-executable instructions for a method comprising:

detecting an event associated with one of said plurality of chips;

generating a timestamp with said local time counter at the time of the occurrence of said detected event, said timestamp being associated with said event;

comparing said event and a normalized form of said timestamp with other events and associated normalized timestamps to determine an order of occurrence;

providing a Time Base selected by said processor, said Time Base being a baseline time value;

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

transmitting each said offset for a local time counter to the chip with which the local time counter is associated;

recording each offset associated with each said local time counter at a location accessible to the chip associated with the local time counter; and

normalizing said timestamp using said offset associated with the local time counter prior to reporting said timestamp and said event to said processor.'

42. (New) The storage medium of claim 41 wherein a software timestamp received from the operating system is associated with said reported event and timestamp.

43. (New) The storage medium of claim 42 wherein said software timestamp is used in determining said order of occurrence of events.